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EE 371

February 12th, 2022

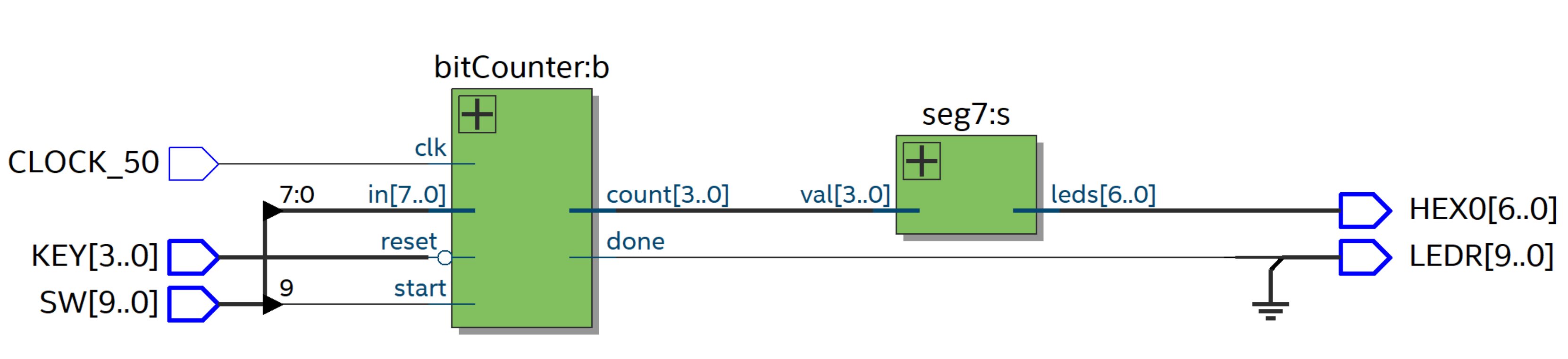
Lab 3 Report

Task1

## Section 1: Procedure

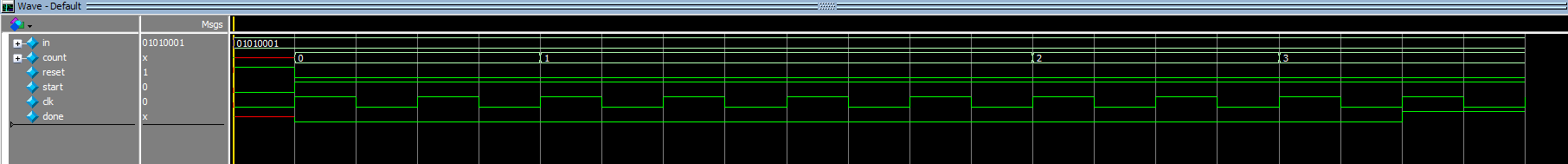
Diagram

Description automatically generated



For the bit counter, I followed the ASMD diagram provided in the lab document. There were 3 states: initial state (S1), count state (S2), and finish state (S3). At the initial state, the counter value is set to 0 and the system loads the input value. Once the start signal is on, the system goes to count state and checks the last digit of the data. If the last digit is 1, counter increases by 1, otherwise it would not change. Then it shifts the data to right by 1. Once the data becomes 0, count finishes and the system stay at finish state until start signal is off.

## Section 2: Results



The waveform shows that the counter goes to 3 and stopped.

## Section 3: Appendix

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Task2

## Section 1: Procedure

Following the ASMD chart in task1, I draw the ASMD chart for task2.

Diagram

Description automatically generated

I designed 4 states, S1: initial state, only load registers, S2: read data from ram and compare with input data, S3: update search address, S4: finish searching. In search state, the system starts with a search boundary from 0 to 31 and compares the current value from the RAM to the value to find. If they are equal, the search finishes. If the current value is larger, the upper bound for the search becomes 1 less than the current address, else the lower bound becomes 1 greater than the current address. Then the system repeats the cycle until it finds the value or the lower bound is larger than or equal to the upper bound, at which the search finishes.

Diagram

Description automatically generated

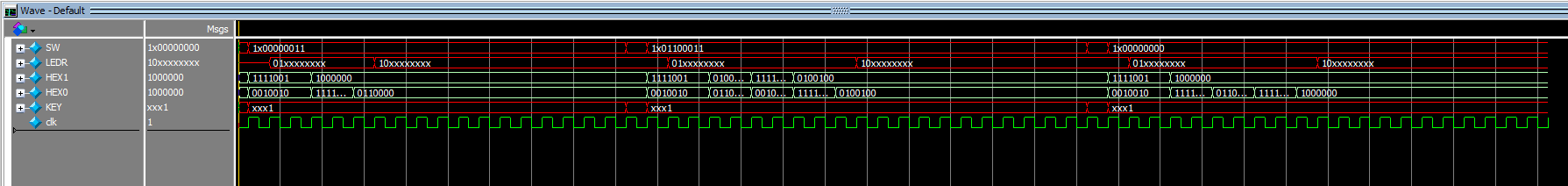
## Section 2: Results

Graphical user interface

Description automatically generated

After a few steps, the system find the target data.

Waveform for DE1\_SoC



## Section 3: Appendix

Table

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Text

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Graphical user interface, text, application

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